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... A **single thread** can initiate a transaction and check ... sections that describe the TestBuilder **multithreading** classes and ... in VHDL and always / initial in **Verilog**. ...

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... thread 4 Simultaneous **Multithreading** (SMT) SMT superior in **single-thread** performance ... **Verilog** simulation is too slow for comprehensive testing Page 27. ...

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Willis, John; Paulsen, William; Abstract. The paper ...

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... Automatic access to Verilog/VHDL state via ... packages to support **testbench** development (mailboxes ... Interactive debugger (including **multi-threading** debug support). ...

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Processor Architecture Laboratory

... For this purpose, the **multi-threaded** tools (graphical debugger, static lock analyzer and system ... You will do experiments with a VHDL **testbench** that includes a ...

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... SPV Software framework for **testbench** automation. ... It works with any Verilog or VHDL simulator via a ... for parallel execution that does not use **multithreading**. ...

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... nor the test code so that when the HDL and the HDL portion of the **testbench** (the SCE-MI ... The transport layer uses the standard **Verilog** PLI or **VHDL** FLI for ...
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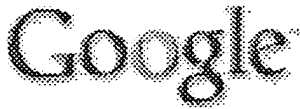

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... use. (VHDL testbench and Verilog design). ... it. One of the nicest features of modelsim (Verilog or VHDL) is the TCL interface. As ...
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